3.3V HIGH-DENSITY SUPERSYNC™ II 36-BIT FIFO

1,024 x 36, 2,048 x 36
4,096 x 36, 8,192 x 36
16,384 x 36, 32,768 x 36

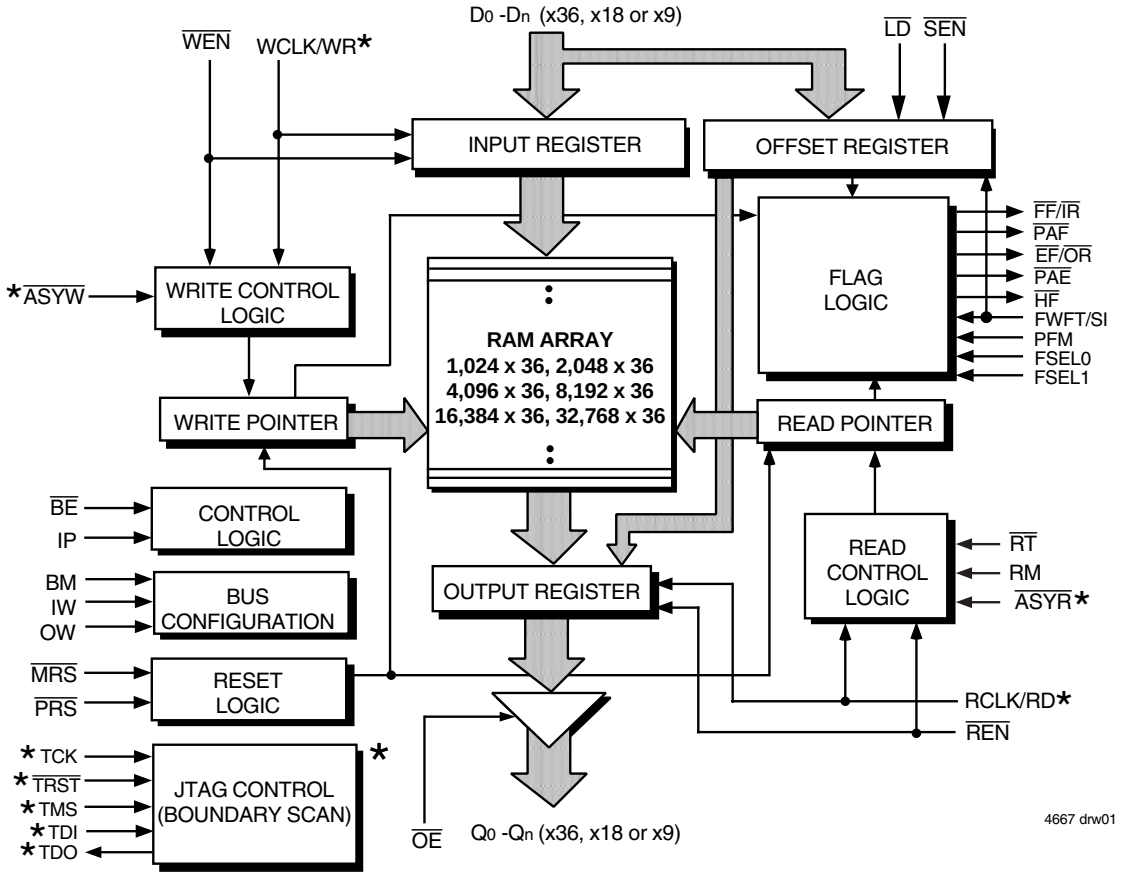
IDT72V3640, IDT72V3650
IDT72V3660, IDT72V3670
IDT72V3680, IDT72V3690

FEATURES:

- Choose among the following memory organizations:
  - IDT72V3640 — 1,024 x 36
  - IDT72V3650 — 2,048 x 36
  - IDT72V3660 — 4,096 x 36
  - IDT72V3670 — 8,192 x 36
  - IDT72V3680 — 16,384 x 36
  - IDT72V3690 — 32,768 x 36
- Up to 166 MHz Operation of the Clocks
- User selectable Asynchronous read and/or write ports (PBGA Only)
- User selectable input and output port bus-sizing
  - *x36 in to x36 out*
  - *x36 in to x18 out*
  - *x36 in to x9 out*
  - *x18 in to x36 out*
  - *x9 in to x36 out*
- Pin to Pin compatible to the higher density of IDT72V36100 and IDT72V36110
- Big-Endian/Little-Endian user selectable byte representation
- 5V input tolerant
- Fixed, low first word latency
- Zero latency retransmit
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty, Full and Half-Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets
- Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags
- Program programmable flags by either serial or parallel means
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Output enable puts data outputs into high impedance state
- Easily expandable in depth and width
- JTAG port, provided for Boundary Scan function (PBGA Only)
- Independent Read and Write Clocks (permit reading and writing simultaneously)
- Available in a 128-pin Thin Quad Flat Pack (TQFP) or a 144-pin Plastic Ball Grid Array (PBGA) (with additional features)
- High-performance submicron CMOS technology
- Industrial temperature range (–40°C to +85°C) is available
- Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAM

***Available on the PBGA package only.**



DESCRIPTION:

The IDT72V3640/72V3650/72V3660/72V3670/72V3680/72V3690 are exceptionally deep, high speed, CMOS First-In-First-Out (FIFO) memories with clocked read and write controls and a flexible Bus-Matching x36/x18/x9 data flow. These FIFOs offer several key user benefits:

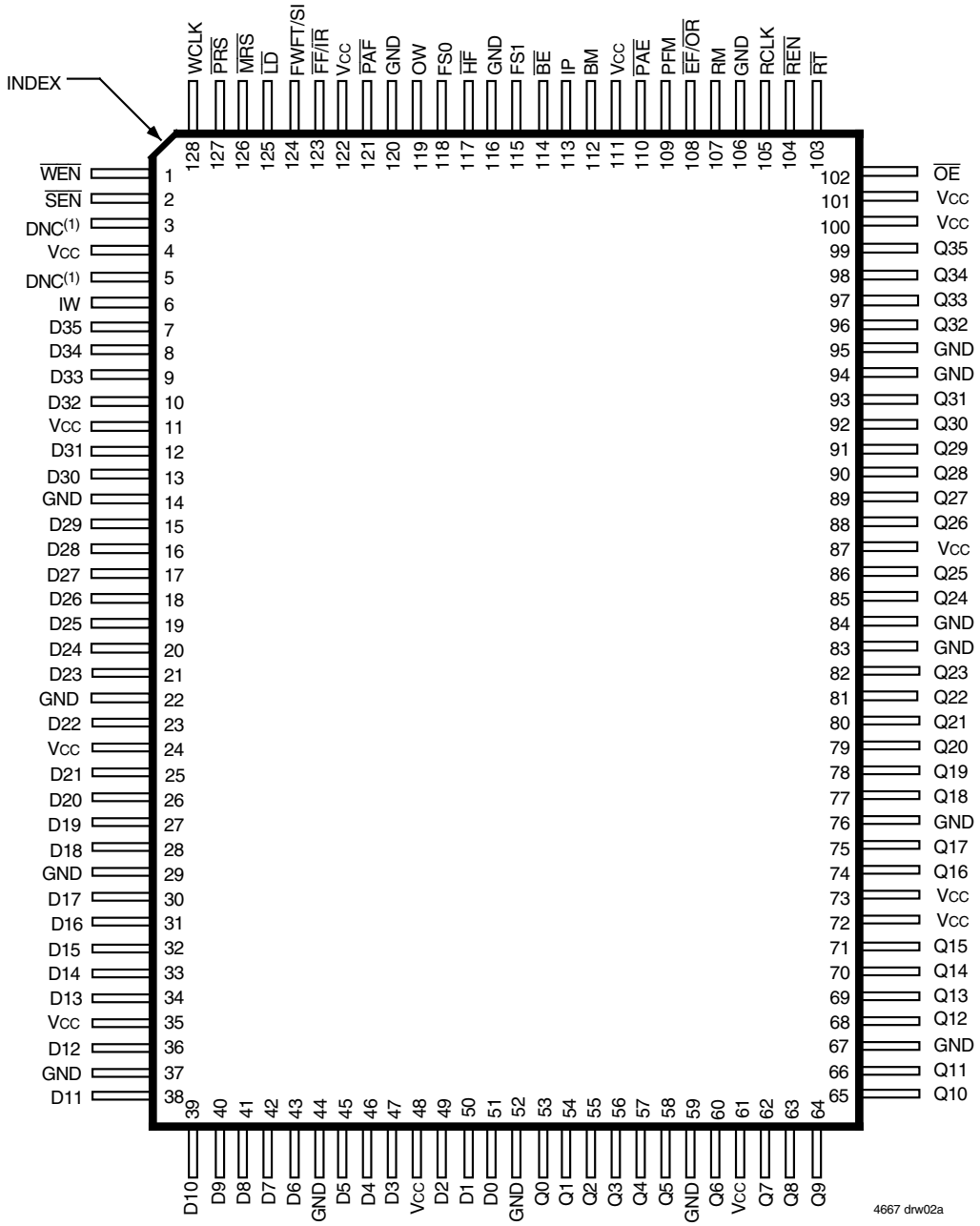
- Flexible x36/x18/x9 Bus-Matching on both read and write ports
- The period required by the retransmit operation is fixed and short.
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.
- Asynchronous/Synchronous translation on the read or write ports
- High density offerings up to 1 Mbit

Bus-Matching Sync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data and match busses of unequal sizes.

Each FIFO has a data input port (D_n) and a data output port (Q_n), both of which can assume either a 36-bit, 18-bit or a 9-bit width as determined by the state of external control pins Input Width (IW), Output Width (OW), and Bus-Matching (BM) pin during the Master Reset cycle.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of

PIN CONFIGURATIONS



TQFP (PK128-1, order code: PF)
TOP VIEW

NOTE:
1. DNC = Do Not Connect.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}[2]	Terminal Voltage with respect to GND	–0.5 to +4.5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}[1]	Supply Voltage Com'l/Ind'l	3.15	3.3	3.45	V
GND	Supply Voltage Com'l/Ind'l	0	0	0	V
V_{IH}[2]	Input High Voltage Com'l/Ind'l	2.0	—	5.5	V
V_{IL}[3]	Input Low Voltage Com'l/Ind'l	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	-40	—	85	°C

NOTES:

1. V_{CC} = 3.3V ± 0.15V, JEDEC JESD8-A compliant.
2. Outputs are not 5V tolerant.
3. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	IDT72V3640L, IDT72V3650L, IDT72V3660L, IDT72V3670L, IDT72V3680L, IDT72V3690L Commercial and Industrial[1] t_{CLK} = 6, 7-5, 10, 15 ns		Unit
		Min.	Max.	
I_{LI}[2]	Input Leakage Current	–1	1	µA
I_{LO}[3]	Output Leakage Current	–10	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	0.4	V
I_{CC1}[4,5,6]	Active Power Supply Current	—	40	mA
I_{CC2}[4,7]	Standby Current	—	15	mA

NOTES:

1. Industrial temperature range product for the 7-5ns and 15ns speed grades are available as a standard device. All other speed grades are available by special order.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs open (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 4.2 + 1.4*fs + 0.002*C_L*fs (in mA) with V_{CC} = 3.3V, t_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1] — SYNCHRONOUS TIMING

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Commercial PBGA & TQFP		Com'l & Ind'l[2] PBGA & TQFP		Commercial TQFP Only		Com'l & Ind'l[2] TQFP Only		
		IDT72V3640L6 IDT72V3650L6 IDT72V3660L6 IDT72V3670L6 IDT72V3680L6 IDT72V3690L6		IDT72V3640L7-5 IDT72V3650L7-5 IDT72V3660L7-5 IDT72V3670L7-5 IDT72V3680L7-5 IDT72V3690L7-5		IDT72V3640L10 IDT72V3650L10 IDT72V3660L10 IDT72V3670L10 IDT72V3680L10 IDT72V3690L10		IDT72V3640L15 IDT72V3650L15 IDT72V3660L15 IDT72V3670L15 IDT72V3680L15 IDT72V3690L15		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Clock Cycle Frequency	—	166	—	133.3	—	100	—	66.7	MHz
t_A	Data Access Time[5]	1	4	1[5]	5	1[5]	6.5	1[5]	10	ns
t_{CLK}	Clock Cycle Time	6	—	7.5	—	10	—	15	—	ns
t_{CLKH}	Clock High Time	2.7	—	3.5	—	4.5	—	6	—	ns
t_{CLKL}	Clock Low Time	2.7	—	3.5	—	4.5	—	6	—	ns
t_{DS}	Data Setup Time	2	—	2.5	—	3.5	—	4	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{ENS}	Enable Setup Time	2	—	2.5	—	3.5	—	4	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{LDS}	Load Setup Time	3	—	3.5	—	3.5	—	4	—	ns
t_{LDH}	Load Hold Time	0.5	—	0.5	—	0.5	—	1	—	ns
t_{RS}	Reset Pulse Width[3]	10	—	10	—	10	—	15	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	15	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	15	—	15	—	15	ns
t_{RTS}	Retransmit Setup Time	3	—	3.5	—	3.5	—	4	—	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid[5]	1	4	1[5]	6	1[5]	6	1[5]	8	ns
t_{OHZ}	Output Enable to Output in High-Z[4,5]	1	4	1[5]	6	1[5]	6	1[5]	8	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	4	—	5	—	6.5	—	10	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	4	—	5	—	6.5	—	10	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	—	10	—	12.5	—	16	—	20	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	4	—	5	—	6.5	—	10	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	—	10	—	12.5	—	16	—	20	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	4	—	5	—	6.5	—	10	ns
t_{HF}	Clock to $\overline{HF}$	—	10	—	12.5	—	16	—	20	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$	4	—	5	—	7	—	9	—	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	5	—	7	—	10	—	14	—	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 7-5ns and 15ns speed grades are available as standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.
5. TQFP package only: for speed grades 7.5ns, 10ns and 15ns, the minimum for t_A, t_{OE}, and t_{OHZ} is 2ns.

AC ELECTRICAL CHARACTERISTICS(1) — ASYNCHRONOUS TIMING

(Commercial: V_{CC} = 3.3V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Commercial		Com'l & Ind'l		
		IDT72V3640L6 IDT72V3650L6 IDT72V3660L6 IDT72V3670L6 IDT72V3680L6 IDT72V3690L6		IDT72V3640L7-5 IDT72V3650L7-5 IDT72V3660L7-5 IDT72V3670L7-5 IDT72V3680L7-5 IDT72V3690L7-5		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_A(4)	Cycle Frequency (Asynchronous mode)	—	100	—	83	MHz
t_{AA}(4)	Data Access Time	0.6	8	0.6	10	ns
t_{CYC}(4)	Cycle Time	10	—	12	—	ns
t_{CYH}(4)	Cycle HIGH Time	4.5	—	5	—	ns
t_{CYL}(4)	Cycle LOW Time	4.5	—	5	—	ns
t_{RPE}(4)	Read Pulse after $\overline{EF}$ HIGH	8	—	10	—	ns
t_{FFA}(4)	Clock to Asynchronous $\overline{FF}$	—	8	—	10	ns
t_{EFA}(4)	Clock to Asynchronous $\overline{EF}$	—	8	—	10	ns
t_{PAFA}(4)	Clock to Asynchronous Programmable Almost-Full Flag	—	8	—	10	ns
t_{PAEA}(4)	Clock to Asynchronous Programmable Almost-Empty Flag	—	8	—	10	ns

NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. Paramaeters apply to the PBGA package only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns(1)
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load for t_{CLK} = 10ns, 15 ns	See Figure 2a
Output Load for t_{CLK} = 6ns, 7.5ns	See Figure 2b & 2c

NOTE:
1. For 166MHz and 133MHz operation input rise/fall times are 1.5ns.

AC TEST LOADS - 6ns, 7.5ns Speed Grades

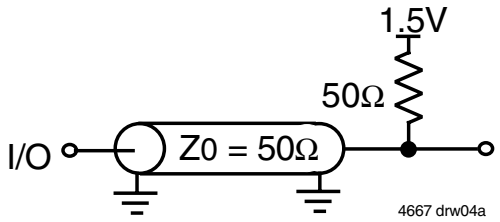


Figure 2b. AC Test Load

AC TEST LOADS - 10ns, 15ns Speed Grades

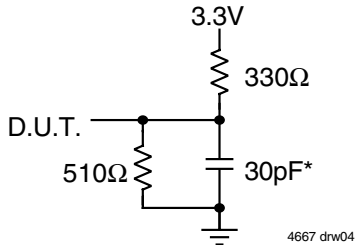


Figure 2a. Output Load
* Includes jig and scope capacitances.

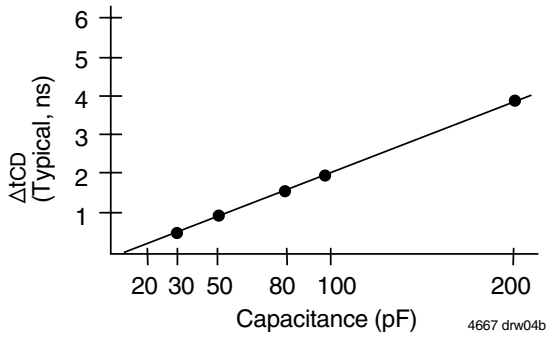
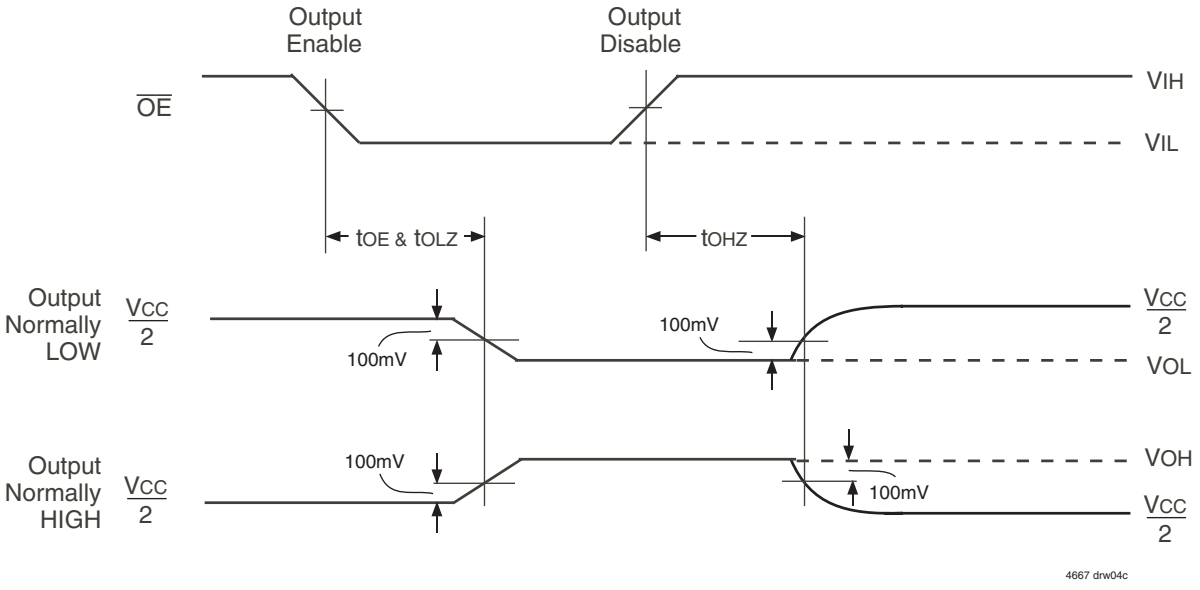


Figure 2c. Lumped Capacitive Load, Typical Derating

OUTPUT ENABLE & DISABLE TIMING



NOTE:
1. $\overline{REN}$ is HIGH.

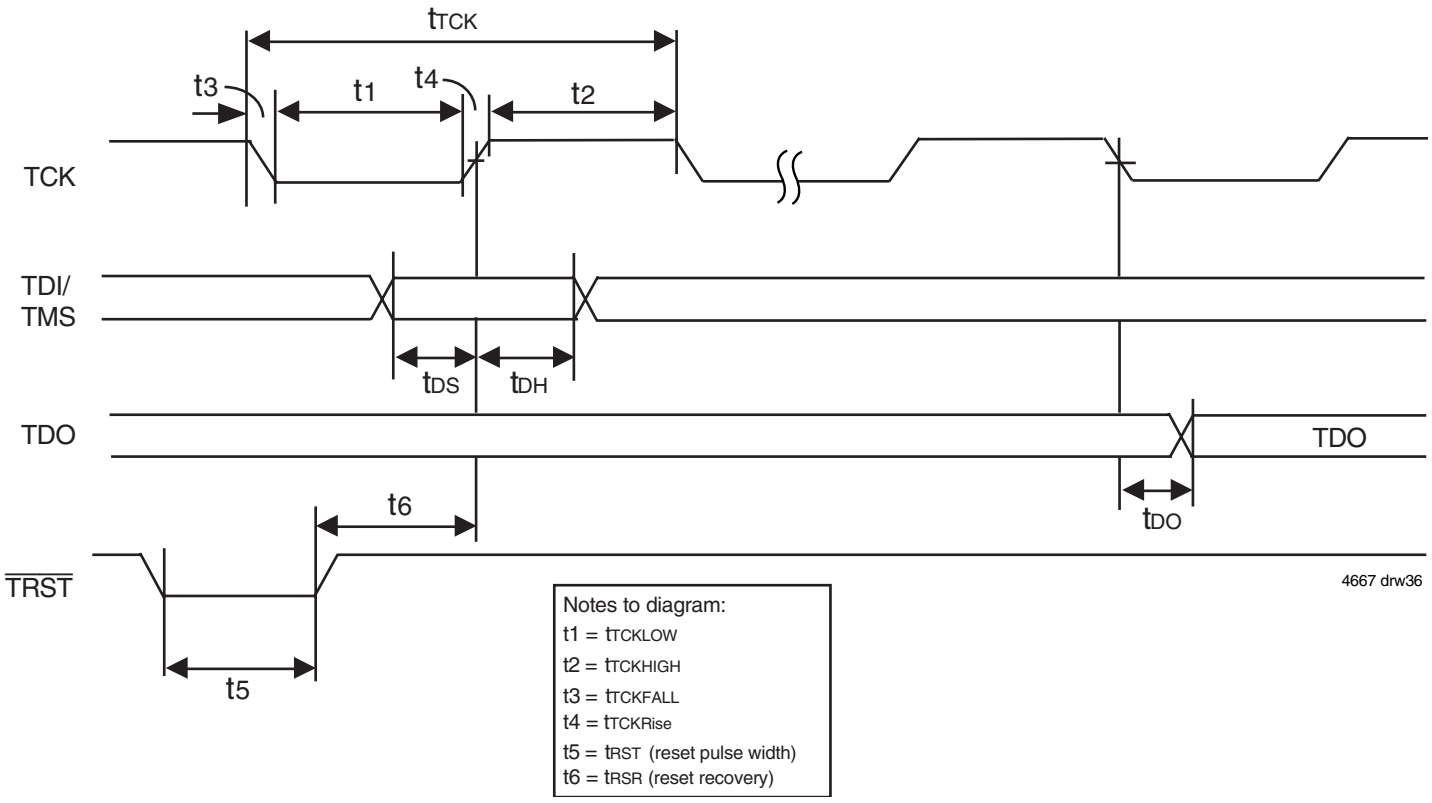


Figure 31. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72V3640 IDT72V3650 IDT72V3660 IDT72V3670 IDT72V3680 IDT72V3690 Min.	Max.	Units
Data Output	t_{DO} = Max		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

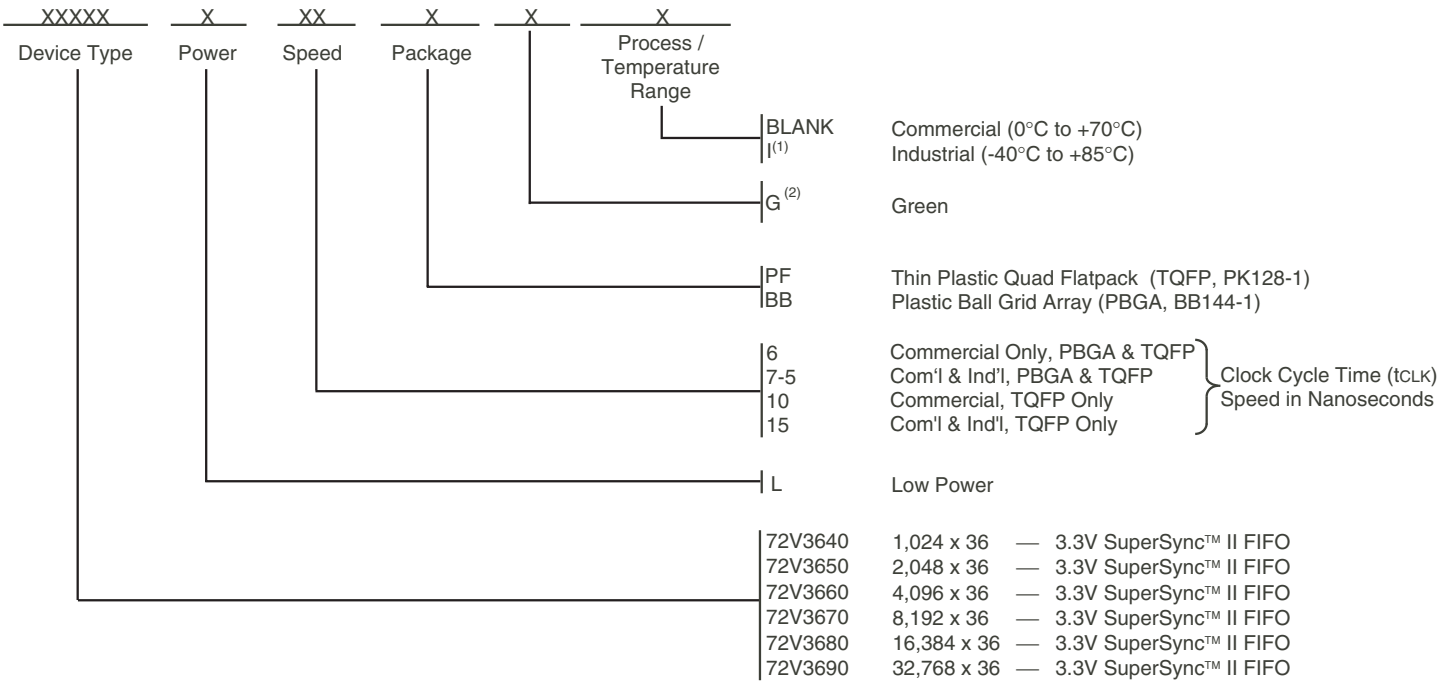
JTAG AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions	Min.	Max.	Units
JTAG Clock Input Period	t_{TCK}	-	100	-	ns
JTAG Clock HIGH	$t_{TCKHIGH}$	-	40	-	ns
JTAG Clock Low	t_{TCKLOW}	-	40	-	ns
JTAG Clock Rise Time	$t_{TCKRise}$	-	-	5[1]	ns
JTAG Clock Fall Time	$t_{TCKFall}$	-	-	5[1]	ns
JTAG Reset	t_{RST}	-	50	-	ns
JTAG Reset Recovery	t_{RSR}	-	50	-	ns

NOTE:
1. Guaranteed by design.

ORDERING INFORMATION



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NOTES:

1. Industrial temperature range product for 7-5ns and 15ns are available as standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact you sales office.